REMARKS

Claim 1 has been amended to emphasize delete the recitation that the sample/latch circuits have inputs that are "**exclusively**" connected to the coding unit (the connection is still recited, but it is no longer recited as being "exclusive"), and to add a recitation that one of the plurality of control signal lines transmits ***a time sequence of the encoded data*** while the other one of the control signal lines transmits ***a time sequence for controlling input/output of the encoded data***. The added limitation is supported by Fig. 4, which shows the time sequences for the control signal line 232 (described in line 16 on page 4 as the data line, meaning that line 232 transmits the encoded data) and control signal line 231 (described in line 15 on page 4 as the "address line," meaning that line 231 controls input and output of encoded data). Because the added recitation is supported by Fig. 4 and page 4, lines 14-16 of the original specification, the additions to not involve "new matter."

Reconsideration of the present patent application is respectfully requested in view of the following remarks.

I. Response to Rejection Under 35 U.S.C. § 112, 1st Paragraph

This rejection has been addressed by amending claim 1 to delete the recitation that the connection between the sample/latch circuit inputs and the coding unit is "exclusive."

II. Response to Rejections Under 35 U.S.C. § 102

The rejection of claims 1, 4, 7, and 9 under 35 U.S.C. §103(a) as being obvious

in view of US Laid Open No. 2003/0085859 (Lee et al.).is respectfully traversed on the grounds that, the Lee publication fails to disclose or suggest that each DA converter is connected to a respective sample/latch circuit by a plurality of control lines, one of which transmits the time sequence of encoded data and the other of which transmits an input/output control time sequence.

As shown, for example, in Figs. 4 and 5 of the Lee publication, the sample/latch units 231, 232, *etc.* of the reference signal generator 200 are connected to D/A converters 600 by a plurality of lines, as claimed.[1] However, the plurality of lines only transmit the outputs of D/A converters 220,250, which supply data sequences and not control sequences. Instead, sequencing of the D/A inputs is provided by an external "sampling start signal" line, shown in Fig. 5, that is not part of the plurality of lines connecting the sample/latch circuits and the D/A converters, while control of the D/A converters is provided by a Polarity Signal line that is also not part of the plurality of lines connecting the sample/latch circuits to D/A converters 600.

The Examiner will note that each sample/latch unit has, as illustrated in Fig. 5 and described in paragraph [0042] of the Lee publication, nine sample/hold circuits, which supply sampled R,G, or B reference data sequences to the D/A converters when triggered by an external "sampling start signal." None of the nine lines is used for control sequences. In contrast, the claimed invention specifically uses the lines connecting the sample/latch circuits to the D/A converters to transmit not only a time sequence of encoded data, but also an input/output control time sequence, so that the external control lines of Lee are not required. The claimed sample-latch circuits simply transmit data received from the coding unit in real time to the D/A converters,

1 The Examiner is correct that Lee teaches a plurality of signal lines in the reference generator. The argument concerning the lack of a plurality of signal lines was the result of a misunderstanding of the Lee publication.

not only without conventional data storage but also without an external timing input, so that the claimed reference voltage generator is, unlike the data drivers of the Lee publication, *independent* of the driving circuit.

As a result of these distinctions, the claimed invention eliminates the need for costly memory and complicated timing arrangements. Because of the use of exclusively-connected sample/latch circuits and a plurality of signal lines, the coding unit of the driving circuit generates a plurality of coded data according to a plurality of characteristic curves at the same time, and the three "separate and regulable" Gamma reference voltages are generated in real time. As a result, during the generation of these three Gamma reference voltages, no storing process is executed, and no "storage device", such as a register" for storing the encoded data, is required. In contrast, as described in paragraph [0026], line 13 to paragraph [0027], line 5 of the specification of the Lee patent, the gamma register 100 receives the digital gamma data through a plurality of data buses from a timing controller (not shown) and stores the digital gamma data in response to the gamma load signal GMA_load, as shown in FIG. 2 of the Lee patent. That is, the gamma register 100 stores the digital gamma data. Therefore, the gamma register 100 does not sample/latch the encoded data (gamma data) during the generation of the reference voltages (gamma reference voltages).

Because the driving circuit of claim 1 of the present patent application is different from the driving circuit of the cited Lee patent in that the lines connecting the sample/latch circuits of the reference generator not only carry data sequences, but also input/output control sequences, withdrawal of the rejection of claim 1 based on the Lee patent is respectfully requested. The other claims included in this rejection

are directly or indirectly dependent on claim 1, and thus are distinguished from the prior art for the same reasons.

CONCLUSION

In view of the foregoing remarks, reconsideration and allowance of the application are now believed to be in order, and such action is hereby solicited. If any points remain in issue that the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

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